MATTHEW NUTT

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EDUCATION

Rice University - Master's in Electrical & Computer Engineering September 2022 - Present
Expected Graduation May 2027 *Houston, TX*

- GPA: 3.88

EXPERIENCE

Electrical Engineering Intern May - August 2025
Lutron Electronics *Austin, TX*

- Developed an auxiliary system to power an RF controller from a solar panel.
- Designed circuit schematics and PCB layouts optimized for low-power energy harvesting and conversion.
- Achieved 20% efficiency in ideal conditions, generating 15× more power than required.

Chief Engineer April 2024 - April 2025
Rice Robotics Club *Houston, TX*

- Assisted in the planning and guidance of a lunar rover project, cat robot project, and BattleBots team, encompassing about 100 individuals from various engineering disciplines.
- Corresponded with team leads on project timelines, technical decisions, and specific team needs.

PROJECTS

FPGA CORDIC Module October 2025

- Implemented the CORDIC trigonometry algorithm with a 16-bit fixed-point datatype in C++, synthesized the module via Vitis HLS and AMD Vivado, and tested the design on an AUP-ZU3 FPGA development board.
- Achieved 360 ns latency with an average deviation of 0.004% from expected results.

Snake Game ASIC May 2025

- Programmed a basic snake game in Verilog, featuring an 8x8 multiplexed display grid, randomly generated apple positions, and dual-phase clocking.
- Verified each module's functionality with dedicated simulation testbenches through QuestaSim.
- Generated layout files for the AMI 0.5 µm PDK from synthesized logic and manually routed I/O to a premade pad frame using Magic to prepare for tapeout.

32-bit Carry-Bypass Adder April 2025

- Used Cadence Virtuoso to construct a schematic-level design of a 32-bit carry-bypass adder for the Skywater 130 nm PDK, with eight bypass units and transistor/gate sizing optimization for each unit.
- Achieved 640 ps critical path delay and 133 µW average power consumption.

Power Supply Supervisor December 2024

- Created a schematic-level ASIC of a power supply supervisor that monitors five voltage rails and generates a synchronous powergood output.
- Designed a 500 kHz PLL circuit in LTSpice that achieved lock in 0.66 ms and produced 0.155% clock jitter.

SKILLS

Programming Languages C/C++, Verilog, Python, MATLAB, Java
Design Tools Cadence Virtuoso and Innovus, Vitis HLS, AMD Vivado, Siemens HyperLynx, Keysight ADS, Magic, KiCad, LTSpice